



**PATENT**

**IN THE U.S. PATENT AND TRADEMARK OFFICE**

Appellants: Young-Doug KIM et al.  
Application No.: 10/737,124  
Art Unit: 2111  
Conf. No.: 5936  
Filed: December 17, 2003  
Examiner: Khanh Dang  
For: AN ARBITER, A SYSTEM AND A METHOD FOR GENERATING  
A PSEUDO-GRANT SIGNAL  
Atty. Dkt. No.: 8947-000074/US

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Mail Stop **Appeal Brief - Patent**

Date: March 23, 2009

**APPELLANT'S BRIEF ON APPEAL UNDER 37 C.F.R. §41.37**

Sir:

This is an Appeal Brief in response to the Final Office Action mailed September 22, 2008 (herein referred to as "Final Rejection" or "FR") and the Notice of Panel Decision from Pre-Appeal Brief Review mailed January 16, 2009 (herein referred to as "Panel Decision"). A Notice of Appeal was filed concurrently with a Pre-Appeal Request for Review on December 22, 2008. Appellant submits herewith their Brief on Appeal as required by 37 C.F.R. §41.37 along with the appropriate governmental fees as required by 37 C.F.R. §41.20(b)(2).

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**I. REAL PARTY IN INTEREST:**

The real party in interest is Samsung Electronics Co., LTD.

**II. RELATED APPEALS AND INTERFERENCES**

No related appeals or interferences are known.

**III. STATUS OF CLAIMS:**

Claims 1-10 and 13-43 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent No. 6,393,506 ("*Kenny*"). Final Rejection at 2.

Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kenny* in view of the following remarks set forth on page 9 of the September 22, 2008 Final Office Action. Final Rejection at 9.

Claims 1-43 are being appealed.

**IV. STATUS OF AMENDMENTS:**

No amendments have been filed subsequent to the Final Rejection.

**V. SUMMARY OF CLAIMED SUBJECT MATTER:**

**A. CONCISE EXPLANATION OF THE SUBJECT MATTER SET FORTH IN EACH INDEPENDENT CLAIM ARGUED SEPARATELY.**

1. A general discussion of the subject matter described in the specification to assist the Board in understanding example embodiments described in the present application.

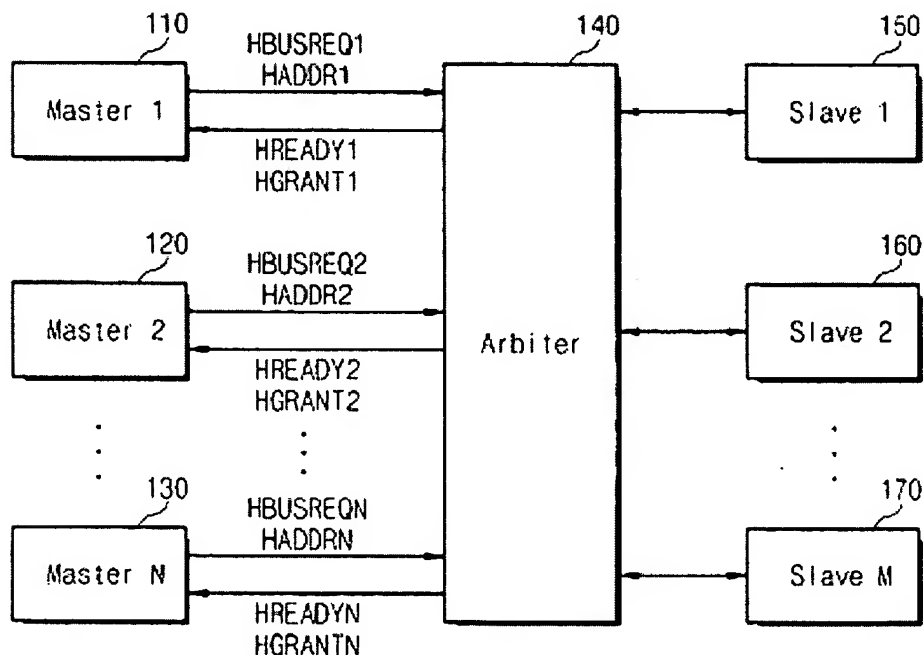
Generally speaking, arbitration mechanisms improve bus bandwidth between at least one master and at least one target slave. Basic operations of known arbitration include a request, arbitration, grant, and data transfer. Specifically, in operation a master requests access to a target slave via an arbitration mechanism. In response, the arbitration mechanism grants bus ownership to the requesting master, and the requesting master transfers data to the target slave via the bus.

Conventionally, grant and data transfer are performed after actual arbitration of the bus. By contrast, example embodiments modify the order of arbitration signals from the conventional order. More specifically, in example embodiments, the pseudo grant signal *precedes* the arbitration. Further, in example embodiments, the target information transfer regarding target slave devices *precedes* the arbitration so that the information contained in the data transfer may be used in the arbitration decision. Example embodiments reduce or eliminate a waiting time T and/or enable better arbitration decisions due to the additional information available for the arbitration.

FIG. 5 of the present application (shown below for the Board's

convenience) illustrates a bus arbitration structure in accordance with an example embodiment.

Fig. 5



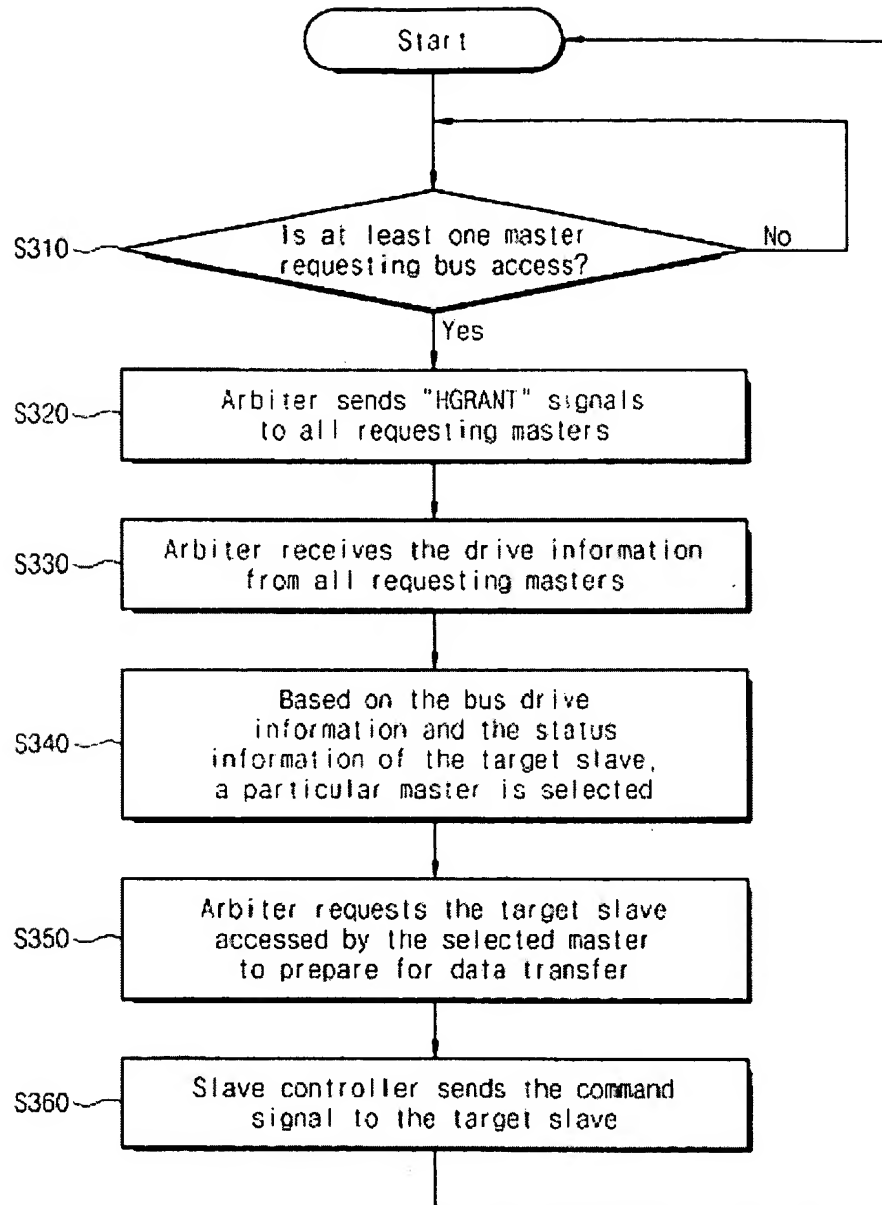
Referring to FIG. 5, the bus arbitration structure includes N master units 110, 120, 130, an arbiter 140, and M slave units 150, 160, 170. In example operation, each master unit 110, 120, 130 sends a request signal HBUSREQN to the arbiter 140. The request signal HBUSREQN is a request signal requesting access to a target slave (e.g., slaves 150, 160, or 170). In response to the request signal HBUSREQN, the arbiter 140 provides a

*pseudo* grant signal HGRANT to each of the N requesting master units 110, 120, 130 at the same time. The *pseudo* grant signal HGRANTN is a signal granting bus ownership to a master. Each of the N master units 110, 120, 130 then provides target information to the arbiter 140 for the arbiter 140 to perform *actual* arbitration of the bus. In the example embodiment illustrated in Figure 5, the target information for the target slave device is the address signal HADDRN. The arbiter 140 performs arbitration and indicates data transfer is ready to occur by providing each master 110, 120 with a ready signal HREADYN.

As noted above, conventionally a grant signal HGRANT is provided *after* actual arbitration of the bus. In example embodiments, however, the *pseudo* grant signal HGRANT is provided after a request, but *prior to actual arbitration of the bus*.

FIG. 11 of the present application (shown below for the Board's convenience) illustrates a flow chart describing a method in accordance with another example embodiment.

Fig. 11



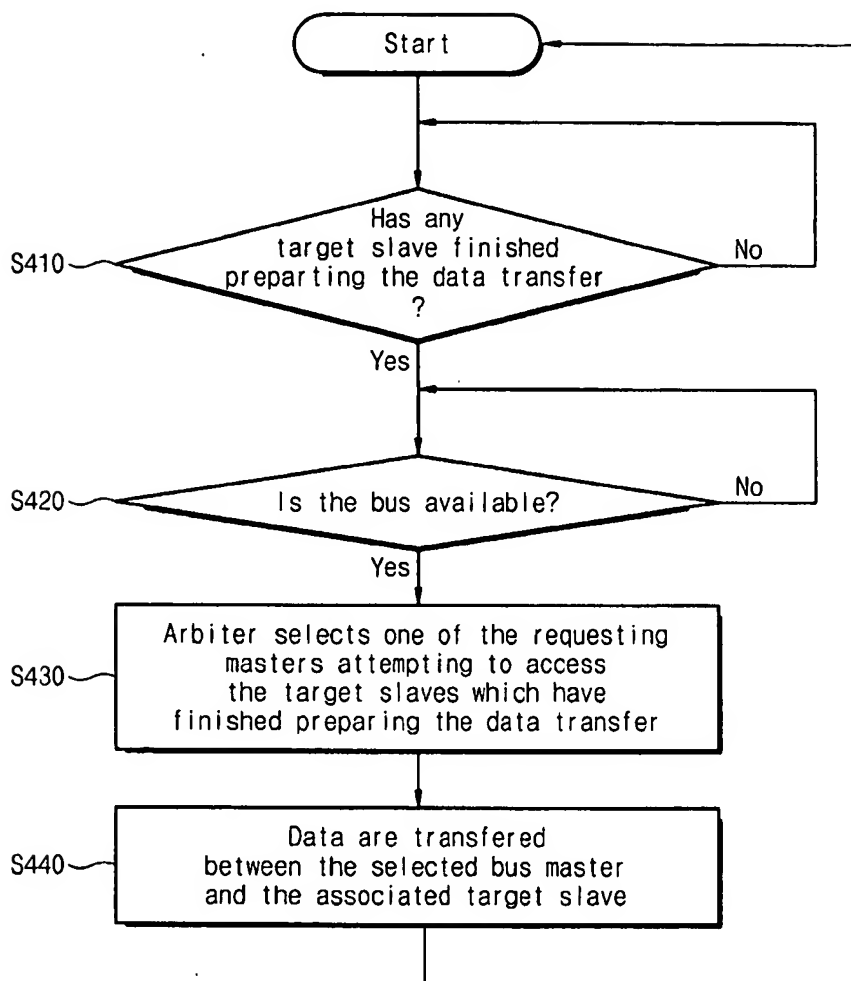
Referring to FIG. 11, at step 310 the arbiter determines whether at least one master is requesting bus access. If not, the arbiter stays in a holding loop. Otherwise, the arbiter sends a pseudo grant signal HGRANT

signal to each requesting master unit at step S320. In response to the received pseudo grant signal HGRANT, the requesting master units send transaction information including drive or target information to the arbitrator.

At step S330, the arbiter receives drive or target information from all requesting master units. At step 340, the arbitrator performs bus arbitration by selecting a particular master based on the transaction information. At step S350, the arbiter requests the target slave accessed by the selected master to prepare for data transfer to reduce latencies associated with the target slave regardless of bus availability. At S360, the slave controller sends the command signal to the target slave.

FIG. 12 (shown below for the Board's convenience) illustrates a second stage of the method.

Fig. 12



Referring to FIG. 12, at step 410 the arbiter determines whether any target slaves have finished preparing for data transfer. If not, the arbiter stays in the holding loop. Otherwise, at step 420 the arbiter determines whether the bus is available. If the bus is not available, the arbiter stays in a holding loop. If the bus is available, at step 430 the arbiter selects one of



the requesting masters attempting to access target slaves which have finished preparing for data transfer. At step 440, data is transferred between the selected bus master and the associated target slave and the process repeats.

As mentioned above, example embodiments modify the order of arbitration signals from the conventional order. In particular, the pseudo grant signal *precedes* actual arbitration of the bus. The target or transaction information transfer also *precedes* actual arbitration of the bus so that the information contained in the data transfer may be used in the arbitration decision.

2. An explanation of the subject matter set forth in each independent claim argued separately referring to the specification and/or the drawings by reference characters in accordance with 37 C.F.R. § 41.37(c)(1)(v).

(a) Claim 1

Claim 1 is directed to an arbiter (e.g., FIG. 5:150, FIG. 7:550, FIG. 8:250) in a system. The arbiter comprises at least one interface (FIG. 7:552, FIG. 8:252) for generating pseudo-grant signals (HGRANTN) to all requesting master units (e.g., FIG. 5:110, 120, 130; FIG. 7:510, 520, 530; FIG. 8:210, 220, 230) beginning at the same time. See, e.g., FIG. 6 and Spec. at p. 10, 4-5. The at least one interface also receives transaction information from all requesting master units in response to the pseudo-

grant signals. *See, e.g.*, Spec. at p. 10, ll. 5-6. The transaction information includes information (e.g., HADDRN) on at least one target slave unit for each requesting master unit. *See, e.g.*, Spec. at p. 10, ll. 5-6. The arbiter performs arbitration based on the information on the target slave unit for each requesting master unit by using the information on the target slave unit for each requesting master unit to determine a priority of bus ownership for the requesting master units. *See, e.g.*, Spec. at p. 8, ll. 4-6.

*(b) Claim 14*

Claim 14 is directed to a system. The system includes at least two master units (e.g., FIG. 5:110, 120, 130; FIG. 7:510, 520, 530; FIG. 8:210, 220,230) for generating a request (e.g., HBUSREQ). *See, e.g.*, Spec. at p. 10, ll. 3-4. An arbiter (e.g., FIG. 5: 150; FIG. 7:550; FIG. 8:250) receives the request from the at least two master units and generates pseudo-grant signals (e.g., HGRANTN) beginning at the same time in response to the request from the at least two master units. *See, e.g.*, FIG. 6 and Spec. at p. 10, ll. 4-5. At least two master units supply target information (e.g., HADDRN) to the arbiter in response to the pseudo-grant signals. *See, e.g.*, Spec. at p. 10, ll. 5-6. At least one slave unit (e.g., FIG. 5:150, 160, 170; FIG. 7:571, 572, 573; FIG. 8: 240) prepares for data transfer in response to the target information supplied by the at least two master units. *See, e.g.*, Spec. at p. 10, ll. 10-13; p. 9, ll. 6-7. The target information includes

information on at least one target slave unit for each requesting master unit. *See, e.g.*, Spec. at p. 10, ll. 5-6. And, the arbiter performs arbitration based on the information on the target slave unit for each requesting master unit by using the information on the target slave unit for each requesting master unit to determine a priority of bus ownership for the requesting master units. *See, e.g.*, Spec. at p. 7, ll. 15-17.

(c) *Claim 19*

Claim 19 is directed to a method of performing arbitration in a system, the method comprising: generating pseudo-grant signals, in response to at least two requests, beginning at the same time (*See, e.g.*, FIG. 11: S320; Spec. at p. 12, ll. 5-6; FIG. 6, Spec. at p. 8, ll. 15-p. 9, ll. 1-4); receiving target information in response to the pseudo-grant signals, the target information including information on at least one target slave unit associated with each request (*e.g.*, FIG. 11: S320; Spec. at p. 12, ll. 5-6); and performing arbitration based on the information on the target slave unit associated with each request by using the information on the target slave unit associated with each request to determine a priority of bus ownership of a plurality of master units generating the at least two requests (*See, e.g.*, FIG. 11: S340; Spec. at p. 12, ll. 7-8).

*(d) Claim 26*

Claim 26 reads on a method of performing arbitration in a system, the method comprising: generating at least two requests (*See, e.g., Spec. at p. 7, ll. 18-19*); receiving the at least two requests and generating pseudo-grant signals in response to the at least two requests beginning at the same time (*See, e.g., FIG. 6; Spec. at p. 8, ll. 1-3*); supplying target information in response to the pseudo-grant signals, the target information including information on at least one target slave unit associated with each request (*See, e.g., Spec. at p. 8, ll. 3-4*); preparing for data transfer in response to the target information (*See, e.g., FIG. 7; Spec. at p. 9, ll. 6-7*); and performing arbitration based on the information on the target slave unit associated with each request by using the information on the target slave unit associated with each request to determine a priority of bus ownership of a plurality of requesting master units generating the at least two requests (*See, e.g., Spec. at p. 8, ll. 4-6*).

*(e) Claim 43*

Claim 43 reads on an arbiter in a system, the arbiter comprising: at least one interface (*e.g., FIG. 7:552; FIG. 8:252*) for generating pseudo-grant signals to all requesting master units beginning at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signals (*See, e.g., FIG. 6; p. 10, ll. 3-5*). Each

of the requesting master units sends a first signal to access a target slave to the at least one interface (*See, e.g.*, Spec. at p. 10, ll. 7-12), the at least one interface generates the pseudo-grant signals beginning at the same time in response to the first signals (*See, e.g.*, FIG. 6), and each of the requesting master units sends the transaction information directly in response to the pseudo-grant signals (*See, e.g.*, Spec. at p. 10, ll. 5-6).

#### **VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL.**

Appellants seek the Board's review of the rejection of claims 1-10 and 13-43 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent No. 6,393,506 ("*Kenny*"). Final Rejection at 2.

Appellants also seek the Board's review of the rejection of claims 11 and 12 under 35 U.S.C. § 103(a) as being unpatentable over *Kenny* in view of the Examiner's remarks on page 9 of the Final Rejection.

**Claims 1-43 are being appealed.**

**Claims 1-13 and 40-42 rise and fall together;**

**Claims 14-18 and 37 rise and fall together;**

**Claims 19-25, 34, and 38 rise and fall together;**

**Claims 26-33, 35 and 39 rise and fall together; and**

**Claim 43 rises and falls alone.**

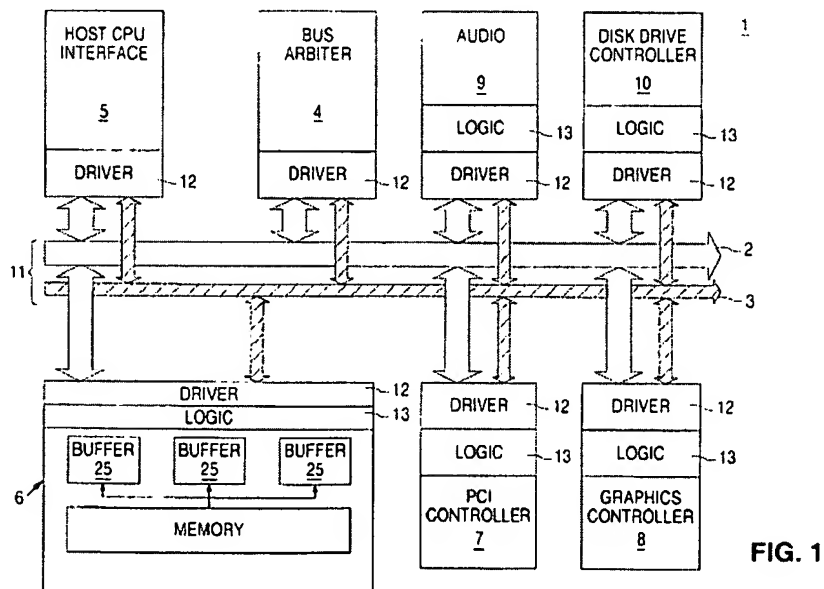
## **VII. ARGUMENT.**

Claims 1-10 and 13-43 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent No. 6,393,506 ("*Kenny*"). Final Rejection at 2. Appellants request the Board overturn this rejection for the following reasons.

### **A. GENERAL DISCUSSION OF KENNY**

*Kenny* discloses a virtual channel bus and system architecture.

FIG. 1 shows a split-transaction bus including a bus arbiter for the virtual channel system according to an embodiment. *Kenny* at 5:27-28.



Referring to FIG. 1, the split-transaction bus 11 includes a data bus 2, an address bus 3, a bus arbiter 4, and functional modules. *Id.* at 5:30-

36. The functional modules include a PCI bus controller 7, a graphics controller 8, an audio module 9, and a disk drive controller 10. *Id.*

FIG. 5 illustrates the operation of system 1 of FIG. 1 in more detail.

*Id.* at 6:62.

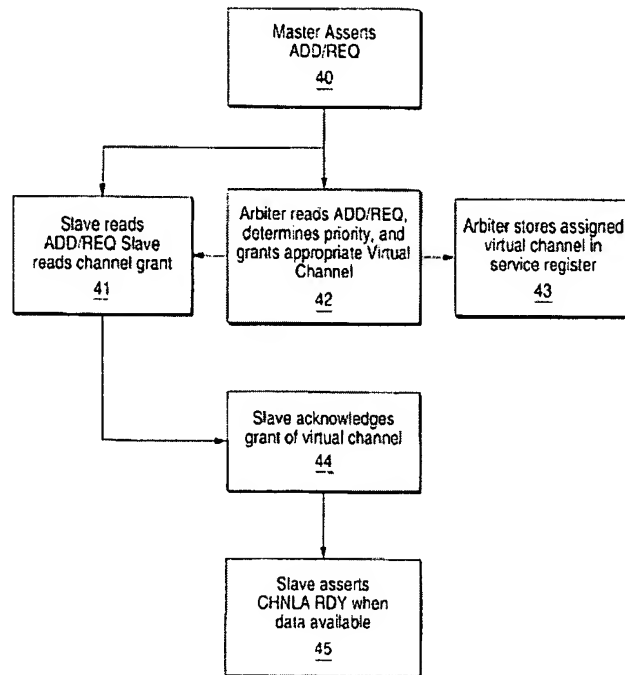


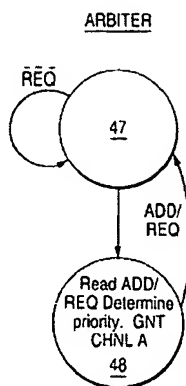
Fig. 5

Referring to FIG. 5, at step 40 a master module (host CPU interface 5) *initializes* bus access by asserting address and bus request signals (ADD/REQ) on the split-transaction bus 11. *Id.* at 62-65. At steps 41 and 42, arbiter 4 and the slave module (memory subsystem 6) detect the address and request signals asserted by the master module 5. *Id.* at 6:65-7:1. Also at step 42, the arbiter 4 identifies the master module making the

request, determines the master module's priority, and grants a virtual channel to the requesting master module. *Id.* at 7:1-3. The granted virtual channel is arbitrarily selected by an allocation procedure. *Id.* at 3-5. Alternatively, each subsystem is configured with a fixed virtual channel having a pre-assigned priority. *Id.* at 5-6.

Still referring to FIG. 5, at step 43 the virtual channel assignment is entered into an "in service" table. *Id.* at 12-13. At step 44, the slave module acknowledges the virtual channel grant. *Id.* at 15-16. In step 45, the slave module asserts a channel ready signal to indicate that it is ready to read data from data bus 2 or to write data onto data bus 2. *Id.* at 16-17.

FIG. 6 shows a state diagram of the virtual channel assignment protocol generally described above in conjunction with FIG. 5. *Id.* at 7:21-23. The portion of FIG. 6 relevant to the arbiter 4 is shown below.



Referring to FIG. 6, in response to detecting a master module's assertion of the address and request signal (ADD/REQ) the arbiter 4 transitions from state 47 to 48. *Id.* at 34-35. The arbiter 4 then asserts



the GNT signal CHNLA on address bus 3 to indicate assignment of a virtual channel ("virtual channel A") to the master module. *Id.* at 36-40. The arbiter 4 assigns the virtual channel according to the master module's preassigned virtual channel and priority or to an allocation procedure. *Id.* After asserting the GNT CHNLA signal, arbiter 4 returns to its initial state 47 to wait for the next address and request signal (ADD/REQ). *Id.* 40-42.

All concurrent virtual channel owners wait for an access grant by arbiter 4 to data bus 2. *Id.* at 57-58. Access to data bus 3 by a particular virtual channel occurs when arbiter 4 asserts the virtual channel's active signal (e.g., CHNLA ACTIVE). *Id.* at 58-60.

**B. KENNY FAILS TO RENDER CLAIM 1 OBVIOUS.**

*Kenny* does not disclose or fairly suggests at least, "*at least one interface for generating pseudo-grant signals ... and for receiving transaction information from all requesting master units in response to the pseudo-grant signals.*" Even further, *Kenny* does not disclose any "*pseudo-grant signal*" whatsoever. Generating "*pseudo-grant signals to all requesting master units beginning at the same time*" as required by claim 1 is also not obvious given the disclosure of *Kenny*.

For at least these reasons, *Kenny* fails to render claim 1 obvious. *In re Lange*, 644 F.2d 856, 862 (CCPA 1981), citing, *Continental Paper Bag Co.*

*v. Eastern Paper Bag Co.*, 210 U.S. 405, 419 (1908); *In re Royka*, 490 F.2d 981, 984, 180 USPQ 580, 582 (CCPA 1974).

1. KENNY FAILS TO DISCLOSE OR FAIRLY SUGGEST "AT LEAST ONE INTERFACE FOR GENERATING PSEUDO-GRANT SIGNALS TO ALL REQUESTING MASTER UNITS BEGINNING AT THE SAME TIME AND FOR RECEIVING TRANSACTION INFORMATION FROM ALL REQUESTING MASTER UNITS IN RESPONSE TO THE PSEUDO-GRANT SIGNALS" AS REQUIRED BY CLAIM 1.

Beginning on page 2, the Final Rejection relies upon the arbiter 4 of *Kenny* to disclose the "arbiter" of claim 1. Specifically, the Final Rejection states, at page 2:

With regard to claim 1, *Kenny* discloses an arbiter (arbiter 4, Fig. 1, for example) in a system (shown generally at Fig.1) for generating a pseudo-grant signal to all requesting master units (the arbiter 4 in *Kenny* "assigns a virtual channel to each master/slave pair requesting the data bus for data transfer between the mater module and a slave module).

Appellants disagree with this conclusion.

Referring again to FIG. 5 of *Kenny*, at step 40 master module 5 initializes bus access by asserting an address and bus request signal (ADD/REQ) on the bus 11. *Kenny* at 6:62-65. According to column 7, lines 22-26, the address portion of the address and bus request signal includes an address of the target slave. *Id.* at 7:22-26. After detecting the address and bus request signals asserted by the master module, the arbiter 4 identifies the master module making the request, determines the master module's priority, and grants a virtual channel at step 42. *Id.* at

7:1-3. Thus, in *Kenny* the master module 5 initializes bus access by asserting an address and bus request signal (ADD/REQ) on the bus 11. Only after receiving the address and bus request signal (ADD/REQ) does the arbiter 4 assert the virtual channel grant signal to the requesting master module 5.

To meet the limitations of claim 1, the arbiter 4 of *Kenny* must "[generate] pseudo-grant signals [and receive] transaction information from all requesting master units *in response to the pseudo-grant signals*." But, as described above this is not the case. Only after receiving the address and bus request signal (ADD/REQ) does the arbiter 4 assert the virtual channel grant signal to the requesting master module 5. *Kenny* does not disclose (either explicitly or implicitly), that the arbiter 4 asserts any signal, let alone a pseudo grant signal, prior to receiving the address and bus request signal (ADD/REQ) from the master module 5.

Indeed, *Kenny* utilizes the term "*initializes*" to refer to the assertion of the address and bus request signal (ADD/REQ) from the master module 5, which indicates this to be the *first or initial step in the process*. The logical conclusion from the use of the term "initialize" is that the master module 5 asserts the address and bus request signals *prior* to receiving any signals from the arbiter 4, let alone, a "pseudo-grant signal."

This conclusion is further supported by FIG. 6 of *Kenny*. As shown in FIG. 6, the arbiter 4 transitions from an initial state 47 to state 48 (in

which a virtual channel grant is asserted) only after receiving the address and bus request signal (including the address of the slave) from the *master module*. *Kenny* at 7:34-40. In other words, FIG. 6 also shows that the address and bus request signal is issued by the master module *prior to* (not after or in response to) the virtual channel grant from the arbiter 4. Indeed, it is the virtual channel grant that is asserted by the arbiter 4 in response to the address and bus request signal from the master module, not vice versa.

Further still, FIG. 9A of *Kenny* also supports that the virtual channel grant is issued only after receiving an address and bus request signal (ADD/REQ) signal from the master module. FIG. 9A (reproduced below) is a timing diagram illustrating operation of virtual channel split-transaction system 1.

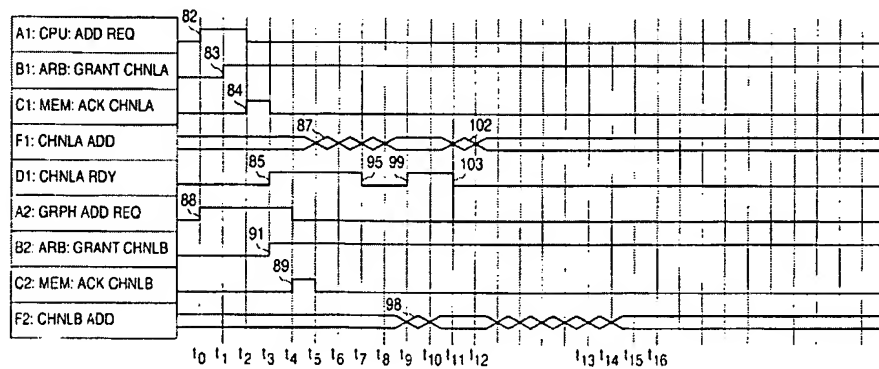


FIG. 9A

FIG. 9

FIG. 9A

FIG. 9B

As *Kenny* states in describing FIG. 9A, the "arbiter 4 ... grants virtual channels A, B and C ...by asserting signal GNT CHLNA, signal GNT

CHLNB, and GNT CHLNC." *Kenny* at 9:53-56. Clearly, one can appreciate from FIG. 9A that the granting of the virtual channels A, B, and C occurs *after* receiving respective address and bus request signals (CPU: ADD REQ and GRPH: ADD REQ) from the requesting master modules CPU and GRPH.

In sum, from review of FIGS. 5, 6 and 9A, one can appreciate that the arbiter 4 of *Kenny* does not receive the address and bus request signal from the master module in response to the virtual channel grant from the arbiter 4. Rather, in *Kenny* the arbiter 4 receives the address and bus request signal prior to asserting the virtual channel grant.

At page 4 of the Final Rejection, the Examiner attempts to distort the teachings of *Kenny* such that claim 1 reads on this reference by directing Appellants' attention to FIG. 6 of *Kenny*. Final Rejection at 4. Specifically, the Examiner states:

*Kenny* also discloses that the arbiter receives transaction information from all requesting master units in response to the pseudo-grant signals (after asserting signal GNT CHNLA, arbiter 4 returns to its initial state 47 to wait for the next ADD/REQ signal from each of the requesting master).

Appellants also disagree with this conclusion.

Referring again to FIG. 6 of *Kenny*, upon detecting the address and bus request signal from the master module, the arbiter 4 asserts grant channel A signal GNT CHNLA on address bus 3 to assign a virtual channel to master module. *Kenny* at 7:34-7:37. After transmitting the virtual grant

channel signal GNT CHNLA, the arbiter 4 returns to its initial state 47 to wait for the next address and bus request signal. *Id.* at 41-42. But, the next address and bus request signal received by the arbiter 4 is from a different master module (see, *Kenny* at FIG. 9A), and therefore, is independent of – not in response to – the grant channel A signal GNT CHNLA from the arbiter 4. Thus, contrary to the Examiner's assertion, the arbiter 4 does not receive the address and bus request signal from a master module 4 in response to the virtual channel grant as required to meet the limitations of claim 1.

The Final Rejection further states, at page 13:

...it is clear from *Kenny*, particularly Fig. 6 [...] that the next ADD/REQ is not independent. As a matter of fact, the next ADD/REQ would not be sent to the master if the GNT without reception of the GNT signal. In other words, ADD/REQ (transaction information) from requesting masters is sent to the arbiter in response to the pseudo-grant signals.

While the above-statement is not completely clear, Appellants believe the underlying assertion is still flawed. Firstly, the address and bus request signal (ADD/REQ) is not sent from the arbiter 4 to the master module 5, but received from the master module 5 by the arbiter 4.

Further, it appears that the above-statement is intended to express that the master module 5 would not send the next address and bus request signal without having first received the grant signal from the arbiter 4. But, such a statement contradicts the initial functionality of *Kenny* in which the address and bus request signal from the master

module initializes bus access, and is sent prior to receiving any virtual channel grant signal from the arbiter 4. *Kenny* does not disclose that the subsequent address and bus request signal (ADD/REQ) is in any way related to (and thus is not in response to) the prior virtual channel grant signal from the arbiter 4.

In sum, at most FIGS. 5 and 6 of *Kenny* disclose that the master modules assert address and bus request signals to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT CHNLC in *Kenny* are provided only after receiving address and bus request signals from respective requesting master modules. By contrast, in claim 1 the at least one interface of the arbiter generates "pseudo-grant signals to all requesting master units," and receives "transaction information from all requesting master units in response to the pseudo-grant signals."

The Examiner further asserts at page 2 of the Final Rejection:

Each virtual channel represents a timeslice on the bus and is owned by a separate master/slave pair, thereby permitting multiple mast/slave pairs to have concurrent ownership of the singular bus" (emphasis added) [...] It is clear that assigning concurrent ownership (bus ownership or bus grant) of a signal data bus to each master by the arbiter before actual arbitration is interpreted as providing a pseudo bus grant signal by the arbiter to each master [...] It is clear that assigning concurrent ownership (bus ownership or bus grant) of a single data bus to each master by the arbiter before actual

arbitration is interpreted as providing a pseudo bus grant signal by the arbiter to each master.

Assuming *arguendo* that assignment of a virtual channel in *Kenny* was similar to the "pseudo grant signal" of claim 1, the arbiter 4 of *Kenny* still does not receive "transaction information from all requesting master units in response to the pseudo-grant signals" as required to meet the limitations of claim 1. As discussed above, the master modules in *Kenny* are not aware of the virtual channels that have been assigned by the arbiter 4 until the arbiter 4 issues a GNT CHNLA (*Kenny* at 9:53-56)<sup>1</sup>, which is provided only after receiving the address and bus request signal from a requesting master module. Therefore, the arbiter of *Kenny* does not receive transaction information in response to pseudo-grant signals as required to meet the limitations of claim 1.

2. "[GENERATING] PSEUDO-GRANT SIGNALS TO ALL REQUESTING MASTER UNITS BEGINNING AT THE SAME TIME" AS REQUIRED BY CLAIM 1 IS NOT OBVIOUS IN VIEW OF KENNY.

On page 4 of the Final Rejection, the Examiner correctly recognizes that *Kenny* does not disclose "*generating pseudo-grant signals to all requesting master units beginning at the same time*" as recited in claim 1. However, the Examiner submits that doing so would have been obvious in

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<sup>1</sup> ("arbiter 4 ... grants virtual channels A, B and C ...by asserting signal GNT CHLNA, signal GNT CHLNB, and GNT CHLNC.")



view of *Kenny*. Specifically, on pages 4 and 5 of the Final Rejection, the Examiner states (emphasis in original):

Although *Kenny* clearly discloses that pseudo-grant signals are generated to all the requesting masters. *Kenny*, as discussed above regarding Fig. 9, does not particularly disclose that the pseudo-grant signals begin at the same time, as claimed in at least Applicant's claim 1[...]

However [...] *Kenny* also disclose that “[a]lternatively, each subsystem may be configured with a fixed virtual channel with a pre-assigned priority.” Pre-designating virtual channels and priorities for each module simplifies processing by eliminating allocation procedures and requiring arbiter 4 to merely match the I/O address of the requesting master module to that master module's pre-assigned virtual channel and pre-assigned priority, referencing a table stored in a register of arbiter 4 or elsewhere.” Thus, it is clear that by using pre-designating virtual channels and priorities for each module, the arbiter 4 does not have to arbitrate between requesting masters having different priority, and assign a virtual channel to a requesting master according to its priority.

The Examiner therefore concludes (emphasis in original):

[...] it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate pseudo-grant signals GNT CHLNA, GNT CHLNB, and GNT CHLNC to all requesting masters beginning at the same time, because by using a fixed virtual channel with a pre-assigned priority for each of the requesting master, the arbiter 4 does not have to arbitrate between masters resulting in generating/providing pseudo-grant signals to all requesting masters at different starting time.

But, the Examiner fails to recognizes that modifying *Kenny* as suggested would change the principle of operation of *Kenny* because the system of *Kenny* issues virtual grant signals sequentially according to priority of the requesting master modules. If *Kenny* were to be modified as

suggested by the Examiner, the virtual channels would no longer be granted according to a master module's priority, thereby significantly changing the principle operation of the system of *Kenny*; namely prioritizing bus ownership. Because the Examiner's suggested modification would change the principle operation of *Kenny*, the teachings of *Kenny* are not sufficient to render claim 1 *prima facie* obvious. MPEP § 2143.01(VI) ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."), *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

### 3. FURTHER ARGUMENTS AGAINST THE EXAMINER'S REJECTION.

Moving forward, on page 12 of the Final Rejection, the Examiner goes on to state in-part (emphasis in original):

...the only difference between the claimed subject matter [and] that of *Kenny* is that *Kenny* does not explicitly disclose that the pseudo-grant signal is provided to each requesting master unit at the same time. As clearly discussed above in the 103 Rejection, by using re-designated virtual channels and priorities for each module, the arbiter 4 does not have to arbitrate between requesting masters having different priority, and assign a virtual channel to a requesting master according to its priority. However, it is important to note that arbitration must also depend from the information from the requesting master. The information from the master includes address of the target and/or priority of the target.

While claim 1 does differ from *Kenny* in that *Kenny* does not disclose "generating pseudo-grant signals to all requesting master units beginning at *the same time*," claim 1 also differs from *Kenny* in other ways as shown above.

Moreover, if the arbiter 4 of *Kenny* need not arbitrate between requesting masters (as suggested by the Examiner), then the arbiter 4 of *Kenny* does not "*perform arbitration based on the information on the target slave unit for each requesting master unit by using the information on the target slave unit for each requesting master unit to determine a priority of bus ownership for the requesting master units*" after generating pseudo-grant signals and receiving transaction information in response to the pseudo-grant signals as is required to meet the limitations of claim 1.

Further still, even assuming *arguendo* that the arbitration performed by the arbiter 4 of *Kenny* depends from the address of the target and/or priority of the target from the requesting master module as suggested by the Examiner (which Appellants do not admit), the address and/or priority of the target slave still does not constitute the "transaction information," of claim 1 because this information is received *prior to the grant of the virtual channel*, but not "*in response to*," the grant of the virtual channel. *Kenny* at 6:63 – 7:4. For at least these additional reasons, *Kenny* fails to render claim 1 obvious.

4. CONCLUSION WITH RESPECT TO CLAIM 1.

For at least the foregoing reasons, Appellants respectfully submit that *Kenny* does not disclose or even fairly suggest all features of claim 1, and thus, fails to render claim 1 obvious. *In re Lange*, 644 F.2d at 862.

**B. KENNY FAILS TO RENDER CLAIMS 2-10, 40, 41, AND 42 OBVIOUS AT LEAST BY VIRTUE OF THEIR DEPENDENCY FROM CLAIM 1.**

Claims 2-13, 40, 41, and 42 depend from independent claim 1. Therefore, these claims are not anticipated or rendered obvious at least by virtue of their dependency.

**C. KENNY FAILS TO RENDER CLAIMS 14-18 AND 37 OBVIOUS.**

Claim 14 requires, "an arbiter for [...] generating pseudo-grant signals beginning at the same time," and "at least two master units supplying target information to the arbiter in response to the pseudo-grant signals." These features are not disclosed or fairly suggested by *Kenny*. Therefore, *Kenny* fails to render claim 14 obvious. *In re Lange*, 644 F.2d at 862.

As discussed above, at most FIGS. 5 and 6 of *Kenny* disclose that a master module asserts the address and bus request signal (ADD/REQ) to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT

CHNLC in *Kenny* are provided only after receiving respective address and bus request signals from respective requesting master modules. By contrast, in claim 14 the arbiter generates "pseudo-grant signals to all requesting master units" and the at least two master units supply "transaction information from all requesting master units *in response to* the pseudo-grant signals." The arbiter 4 of *Kenny* surely cannot be said to receive transaction information in response to a pseudo-grant signal if the arbiter 4 does not assert any virtual channel grant signal prior to receiving the address and bus request signal from the master module.

Further, as discussed above with regard to claim 1, modifying *Kenny* such that the virtual channel grant signals are generated at the same time would change the principle operation of the system of *Kenny*; namely prioritizing bus ownership. Because the Examiner's suggested modification would change the principle operation of *Kenny*, the teachings of *Kenny* are not sufficient to render claim 14 *prima facie* obvious. MPEP § 2143.01(VI), *In re Ratti*, 270 F.2d 810.

For at least the foregoing reasons, *Kenny* fails to render claim 14 obvious. *Kenny* fails to render claims 16-18 and 37 obvious at least by virtue of their dependency from claim 14.

**D. KENNY FAILS TO RENDER CLAIMS 19-25, 34, AND 35 OBVIOUS.**

Claim 19 requires, "generating pseudo-grant signals [...] beginning at the same time[,] and receiving target information in response to the pseudo-grant signals." These features are not disclosed or fairly suggested by *Kenny*. Therefore, *Kenny* fails to render claim 19 obvious. *In re Lange*, 644 F.2d at 862.

Again as discussed above, at most FIGS. 5 and 6 of *Kenny* disclose that a master module asserts the address and bus request signal (ADD/REQ) to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT CHNLC in *Kenny* are provided only after receiving respective address and bus request signals from respective requesting master modules. By contrast, in claim 19, "pseudo-grant signals" are generated and then "target information" is received "in response to the pseudo-grant signals." The arbiter 4 of *Kenny* surely cannot be said to receive target information on at least one target slave unit in response to a pseudo-grant signal if the arbiter 4 does not assert any virtual channel grant signal prior to receiving the address and bus request signal from the master module.

Further, as discussed above with regard to claim 1, modifying *Kenny* such that the virtual channel grant signals are generated at the same time

would change the principle operation of the system of *Kenny*; namely prioritizing bus ownership. Because the Examiner's suggested modification would change the principle operation of *Kenny*, the teachings of *Kenny* are not sufficient to render claim 19 *prima facie* obvious. MPEP § 2143.01(VI), *In re Ratti*, 270 F.2d 810.

For at least the foregoing reasons, *Kenny* fails to render claim 19 obvious. *Kenny* fails to render claims 20-25, 34, and 38 obvious at least by virtue of their dependency from claim 19.

**E. KENNY FAILS TO RENDER CLAIMS 26-33, 35, AND 39 OBVIOUS.**

Claim 26 requires "generating pseudo-grant signals in response to the at least two requests beginning at the same time" and "supplying target information in response to the pseudo-grant signals." These features are also not disclosed or fairly suggested by *Kenny*. Therefore, *Kenny* fails to render claim 26 obvious. *In re Lange*, 644 F.2d at 862.

At most FIGS. 5 and 6 of *Kenny* disclose that a master module asserts the address and bus request signal (ADD/REQ) to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT CHNLC in *Kenny* are provided only after receiving respective address and bus request signals from respective requesting master modules. By contrast, in claim

26, "pseudo-grant signals" are generated and "target information" is supplied "in response to the pseudo-grant signals." The arbiter 4 of *Kenny* surely cannot be said to receive target information on at least one target slave unit in response to a pseudo-grant signal if the arbiter 4 does not assert any virtual channel grant signal prior to receiving the address and bus request signal from the master module.

Further, as discussed above with regard to claim 1, modifying *Kenny* such that the virtual channel grant signals are generated at the same time would change the principle operation of the system of *Kenny*; namely prioritizing bus ownership. Because the Examiner's suggested modification would change the principle operation of *Kenny*, the teachings of *Kenny* are not sufficient to render claim 26 *prima facie* obvious. MPEP § 2143.01(VI), *In re Ratti*, 270 F.2d 810.

For at least the foregoing reasons, *Kenny* fails to render claim 26 obvious. *Kenny* fails to render claims 27-33, 35, and 39 obvious at least by virtue of their dependency from claim 26.

**F. KENNY FAILS TO RENDER CLAIM 43 OBVIOUS.**

Claim 43 requires "at least one interface for generating pseudo-grant signals to all requesting master units beginning at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signals." This feature is not disclosed or



fairly suggested by *Kenny*. Therefore, *Kenny* fails to render claim 43 obvious. *In re Lange*, 644 F.2d at 862.

As repeatedly stated above, at most FIGS. 5 and 6 of *Kenny* disclose that a master module asserts the address and bus request signal (ADD/REQ) to initialize the master module's bus access and prior to receiving any virtual channel grant signal from the arbiter 4. Moreover, FIG. 9A clearly shows that the virtual channel grants GNT CHNLA, GNT CHNLB, and GNT CHNLC in *Kenny* are provided only after receiving respective address and bus request signals from respective requesting master modules. By contrast, in claim 43, the arbiter includes "at least one interface for generating pseudo-grant signals to all requesting master units beginning at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signals." The arbiter 4 of *Kenny* surely cannot be said to receive transaction information on at least one target slave unit in response to a pseudo-grant signal if the arbiter 4 does not assert any virtual channel grant signal prior to receiving the address and bus request signal from the master modules.

Further, as discussed above with regard to claim 1, modifying *Kenny* such that the virtual channel grant signals are generated at the same time would change the principle operation of the system of *Kenny*; namely prioritizing bus ownership. Because the Examiner's suggested modification would change the principle operation of *Kenny*, the teachings

of *Kenny* are not sufficient to render claim 43 *prima facie* obvious. MPEP § 2143.01(VI), *In re Ratti*, 270 F.2d 810.

For at least the foregoing reasons, *Kenny* fails to render claim 43 obvious.

**G. CLAIMS 11 AND 12 ARE NOT RENDERED OBVIOUS BY KENNY.**

The Examiner rejects claims 11-12 as unpatentable over *Kenny* in view of the Examiner's citation of Wikipedia and the comments set forth on pages 9 and 10 of the Final Rejection. Appellants continue to challenge the Examiner's citation of Wikipedia as sufficient teaching to establish that a particular teaching was well-known in the art at the time of the invention. Wikipedia is an open content encyclopedia the contents of which can be edited by anyone. Moreover, Appellants also challenge the Examiner's mere comments or Official Notice on page 9 of the Final Rejection that the features of claims 11 and 12 would have been obvious. Regardless, however, claims 11 and 12 are patentable by virtue of their dependency from claim 1.

**VIII. CLAIMS APPENDIX.**

An appendix containing a copy of the claims involved in the appeal is attached.

**IX. EVIDENCE APPENDIX.**

An appendix containing copies of any evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the Examiner is attached.

**X. RELATED PROCEEDINGS APPENDIX.**

An appendix containing copies of decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of this section is attached.

**CONCLUSION**

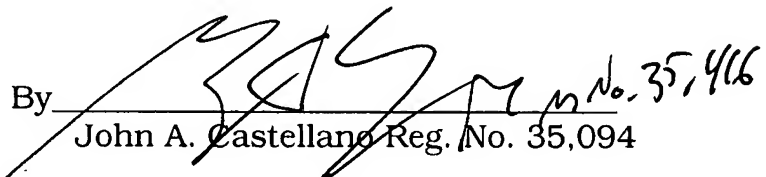
In light of the foregoing arguments, Appellant respectfully requests the Board to reverse the Examiner's rejection of claims 1-10 and 13-43.

The Commissioner is authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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### **VIII. CLAIMS APPENDIX.**

#### **Claims on Appeal:**

1. (Previously Presented) An arbiter in a system, the arbiter comprising:

at least one interface for generating pseudo-grant signals to all requesting master units beginning at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signals, wherein

the transaction information includes information on at least one target slave unit for each requesting master unit, and

the arbiter performs arbitration based on the information on the target slave unit for each requesting master unit by using the information on the target slave unit for each requesting master unit to determine a priority of bus ownership for the requesting master units.

2. (Previously Presented) The arbiter of claim 1, the arbiter further performing arbitration based on the transaction information received from all the requesting master units.

3. (Previously Presented) The arbiter of claim 1, the at least one interface including a master interface for generating the pseudo-grant signals to all

the requesting master units, for receiving the transaction information from all the requesting master units in response to the pseudo-grant signals, and for generating a ready signal to a selected one of the requesting master units.

4. (Original) The arbiter of claim 3, the master interface including at least one generator for generating the pseudo-grant signals from at least one request signal from all the requesting master units.

5. (Previously Presented) The arbiter of claim 3, the master interface including at least one circuit for converting a target slave ready signal from at least one slave of the at least one target slave into a data transfer ready signal for a selected one of the requesting master units.

6. (Original) The arbiter of claim 3, wherein the ready signal is for data transfer.

7. (Original) The arbiter of claim 3, wherein the ready signal indicates bus availability.

8. (Previously Presented) The arbiter of claim 1, the at least one interface including a controller interface for requesting at least one slave unit to

prepare for data transfer in response to the transaction information from the selected one of the requesting master units.

9. (Original) The arbiter of claim 8, wherein the controller interface is a slave controller interface which interacts with at least one slave controller of the at least one slave unit.

10. (Original) The arbiter of claim 9, wherein each slave controller controls at least one slave memory.

11. (Original) The arbiter of claim 8, wherein the controller interface is an SDRAM controller interface which interacts with at least one SDRAM controller of the at least one slave unit.

12. (Original) The arbiter of claim 11, wherein each SDRAM controller controls at least one SDRAM memory bank.

13. (Original) The arbiter of claim 1, wherein a request from all the requesting master units is synchronized with a system clock.

14. (Previously Presented) A system comprising:  
at least two master units for generating a request;

an arbiter for receiving the request from the at least two master units and for generating pseudo-grant signals beginning at the same time in response to the request from the at least two master units;

the at least two master units supplying target information to the arbiter in response to the pseudo-grant signals; and

at least one slave unit preparing for data transfer in response to the target information supplied by the at least two master units, and wherein

the target information includes information on at least one target slave unit for each requesting master unit, and

the arbiter performs arbitration based on the information on the target slave unit for each requesting master unit by using the information on the target slave unit for each requesting master unit to determine a priority of bus ownership for the requesting master units.

15. (Previously Presented) The system of claim 14, wherein the at least one slave unit completes preparing for data transfer and data is transferred between one of the at least two master units and one of the at least one slave units.

16. (Previously Presented) The system of claim 14, wherein all requesting master units in the system receive the pseudo-grant signals from the arbiter.



17. (Previously Presented) The system of claim 14, wherein the request from the at least two master units is synchronized with a system clock.

18. (Previously Presented) The system of claim 14, wherein the pseudo-grant signals from the arbiter and the target information from the at least two master units are synchronized.

19. (Previously Presented) A method of performing arbitration in a system, comprising:

generating pseudo-grant signals, in response to at least two requests, beginning at the same time, and

receiving target information in response to the pseudo-grant signals, the target information including information on at least one target slave unit associated with each request, and

performing arbitration based on the information on the target slave unit associated with each request by using the information on the target slave unit associated with each request to determine a priority of bus ownership of a plurality of master units generating the at least two requests.

20. (Original) The method of claim 19, further comprising:

performing arbitration based on the target information.

21. (Previously Presented) The method of claim 19, wherein the at least two requests and the target information are from the plurality of master units.

22. (Previously Presented) The method of claim 19, wherein the pseudo-grant signals are generated in response to all requests.

23. (Original) The method of claim 19, further comprising:  
requesting preparation for data transfer in response to the target information.

24. (Original) The method of claim 19, wherein the request is synchronized with a system clock.

25. (Previously Presented) The method of claim 19, wherein the method is hardware implemented.

26. (Previously Presented) A method of performing arbitration in a system, comprising:

generating at least two requests;

receiving the at least two requests and generating pseudo-grant signals in response to the at least two requests beginning at the same time;

supplying target information in response to the pseudo-grant signals, the target information including information on at least one target slave unit associated with each request;

preparing for data transfer in response to the target information; and

performing arbitration based on the information on the target slave unit associated with each request by using the information on the target slave unit associated with each request to determine a priority of bus ownership of a plurality of requesting master units generating the at least two requests.

27. (Previously Presented) The method of claim 26, wherein the at least two requests and the target information are from the plurality of requesting master units.

28. (Original) The method of claim 27, further comprising:

completing preparation of data transfer; and  
transferring data.

29. (Previously Presented) The method of claim 28, wherein said generating, receiving, supplying, and preparing constitute a first stage and

said completing and transferring constitute a second stage and said first and second stages occur concurrently.

30. (Original) The method of claim 29, wherein completing preparation of data transfer includes determining whether a bus is available and selecting one of the requesting masters.

31. (Previously Presented) The method of claim 26, wherein the pseudo-grant signals are generated in response to all requests.

32. (Original) The method of claim 26, wherein the request is synchronized with a system clock.

33. (Previously Presented) The method of claim 26, wherein the method is hardware implemented.

34. (Previously Presented) A computer-readable medium containing instructions which, when executed, causes a machine to perform the method of claim 19.

35. (Previously Presented) A computer-readable medium containing instructions which, when executed, causes a machine to perform the method of claim 26.

36. (Previously Presented) The arbiter of claim 1, wherein the at least one interface generates the pseudo-grant signals to all requesting master units at the same time prior to arbitration.

37. (Previously Presented) The system of claim 14, wherein the arbiter generates the pseudo-grant signals to all requesting master units at the same time prior to arbitration.

38. (Previously Presented) The method of claim 19, wherein the pseudo-grant signals are generated at the same time prior to arbitration.

39. (Previously Presented) The method of claim 26, wherein the pseudo-grant signals are generated at the same time prior to arbitration.

40. (Previously Presented) The method of claim 1, wherein the arbiter does not perform the arbitration based on priorities pre-assigned to the master units and does not perform the arbitration based on priorities received from the master units.

41. (Previously Presented) The method of claim 1, wherein the arbiter performs the arbitration based only on the information on the target slave for each requesting master and status information for each of the target slaves.

42. (Previously Presented) The method of claim 1, wherein the arbiter performs the arbitration based on the transaction information, the transaction information being received in response to the pseudo grant signals, the pseudo grant signals being received before the transaction information.

43. (Previously Presented) An arbiter in a system, the arbiter comprising:  
at least one interface for generating pseudo-grant signals to all requesting master units beginning at the same time and for receiving transaction information from all requesting master units in response to the pseudo-grant signals, wherein

each of the requesting master units sends a first signal to access a target slave to the at least one interface,

the at least one interface generates the pseudo-grant signals beginning at the same time in response to the first signals, and

each of the requesting master units sends the transaction information directly in response to the pseudo-grant signals.

**IX. EVIDENCE APPENDIX.**

None.



**X. RELATED PROCEEDINGS APPENDIX.**

None.